REMARKS

Claims 1-30 are pending. The Examiner has maintained the 35 U.S.C. 112 rejection of the phrase "substantially all multi-byte aligned branch instructions." The Examiner has rejected claims 1-11, and 13-29 under 35 U.S.C. 102(b) as being anticipated by Intel (IA-32® Architecture Software Developer's Manual, Volumes 1-2, 2002) and has also cited the Intel article "Data Alignment when Migrating to 64-Bit Intel Architecture."

The Examiner objected to claims 1-13 under 35 U.S.C. 112(2) as being indefinite because of the phrase in independent claim 1 "substantially all multi-byte aligned branch instructions." The language in independent claim 1 and the use of the term "substantially" is believed proper. One of skill in the art would recognize what branch instructions are in light of the specification. For example, branch instructions include "branch on equal or branch on not equal, and jump instructions." (Page 6, lines 7-8) "The branch instructions such as branch on equal or branch on not equal instructions allow a change in the flow of execution of a program by jumping to a nonsequential instruction at a branch target address." (page 6, lines 27-29) One of skill in the art would recognize that an instruction set typically includes a "group of multi-byte aligned branch instructions." The group member can vary depending on the particular architecture. For example, branch instructions may include multi-byte aligned branch on equal, branch on not equal, branch on greater than, branch on less than, branch if equal to 0, branch based on contents of a register, unconditional jump, jump to a register address, etc.

Claim 1 includes the recitation "substantially all multi-byte aligned branch instructions." Requiring all multi-byte aligned branch instructions is believed to be inappropriate, as a potential infringer could easily design around by adding an extraneous multi-byte aligned instruction or a multi-byte aligned test instruction that does not perform claim recitations. The extraneous instruction may be completely frivolous, but would prevent infringement of a claim requiring something of "all multi-byte aligned branch instructions." One of skill in the art would understand the phrase "substantially all multi-byte aligned branch instructions." It is not necessary to define a particular threshold (e.g. 23 out of 25 multi-byte aligned instructions or 92%) as meeting the criteria for substantially. See *Andrew Corp. v. Gabriel Electronics*, 847 F.2d 819, 6 USPQ2d 2010 (Fed. Cir. 1988).

The Examiner has rejected claims 1-11, and 13-29 under 35 U.S.C. 102(b) as being anticipated by Intel (IA-32® Architecture Software Developer's Manual, Volumes 1-2, 2002) and has also cited the Intel article "Data Alignment when Migrating to 64-Bit Intel Architecture."

Claim 1 has been amended to recite "wherein the circuitry is operable perform sign extensions of immediate fields in non-branch instructions and perform sign extensions of immediate fields in branch instructions to calculate a target address for branch instructions."

Claim 14 has been amended to recite "wherein common subcircuitry performs a sign extension of an is used to process the immediate field associated with one or more branch instructions and one or more non-branch instructions, wherein the sign extension of the immediate field associated with one or more branch instruction is performed to determine a branch target address."

Claims 20 and 27 have been amended to recite calculating a branch target address by determining a sign extended value of the immediate value, wherein the branch target address is determined by using common subcircuitry, ... wherein the common subcircuitry is also operable to determine sign extended values of immediate values of non-branch operations;

These amendments are supported in Figures 3-5 and associated description. For example, "Because both branch and non-branch operations perform a sign extended operation on the immediate field value, the same subcircuit can be reused for both types of operations. Using the same subcircuitry allows efficient use of hardware resources and reduced processor core sizes." (page 12, lines 24-27)

Furthermore, "In typical instances, calculating a branch target involves determining the sign extended value of an immediate field associated with a branch instruction. A processor already has other non-branch instructions that perform calculations using the sign extended value of the same immediate field. However, multi-byte alignment issues have conventionally prevented the use of the same subcircuitry to perform both types of instructions. By choosing the branch offset to be in bytes, the same subcircuitry used to perform the sign extension of the immediate field for non-branch instructions can be reused for branch instructions." (page 7, lines 16-23)

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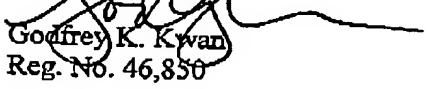
No circuitry or subcircuitry described in any reference teaches or suggests using common subcircuitry to both calculate a branch target address by determining a sign extended value of the immediate value for branch operations and to determine sign extended values of immediate values of non branch operations.

The Examiner argues that an ALU or a decoder could be this common subcircuitry. However, neither the ALU nor the decoder perform a sign extension of the immediate field for non-branch instructions and a sign extension of the immediate field to calculate a branch target address for branch instructions.

In devices such as ASICs or Intel processors, it is less expensive to create a whole new set of branch instructions than it is to modify multi-byte branch instructions to access instructions at byte aligned addresses. "By adding a whole set of new branch instructions, additional subcircuitry will have to be introduced, potentially increasing hardware costs." (page 8, lines 7-9) "In many processors and ASICs, adding logic and subcircuitry to handle unique instructions is less-expensive than adding logic in a programmable chip to handle unique instructions." (page 9, lines 28-30)

In light of the above remarks, the rejections to the independent claims are believed overcome for at least the reasons noted above. Applicants believe that all pending claims are allowable in their present form. Please feel free to contact the undersigned at the number provided below if there are any questions, concerns, or remaining issues.

Respectfully submitted,
BEYER WEAVER, LLP



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